RELIABILITY INVESTIGATION ON S- Band GaAs MMIC

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Abstract

Accelerated life tests and radiation hardness tests have been conducted on GaAs MMICs and the constituent elements. 0.35 to 1.3 x10^8 hours MTF (Median Time to Failure) at 130°C Tch were estimated for a wide band amplifier up to S-band. No failure has been observed on RF operation tests for 3000 hours at Tch of 180°C and 205°C values for 12 samples, respectively. No degradation in the electrical performemce was observed up to 1 x 10^7 rad gamma-ray irradiation with 5% criteria for the the S-band two-stage amplifiers, two-modulus prescalers and their FETs. It has been confirmed that the MMICs produced, using NEC's 0.8 μm long T-shaped WSi gate FET manufacturing process, are sufficiently reliable for practical applications.

Introduction

GaAs MMIC commercial products were put into microwave communications and measurement system markets a few years ago after a ten year R & D period. The R & D has been becoming more active in semiconductor device suppliers because of the forseen advantages such as compact size, light weight, high productivity and reliability. GaAs MMICs reliability studies have been reported in a few reports,[1] even though it is a key point to be widely introduced in many kinds of systems. In this paper, newly developed GaAs FET is described from the reliability points of view. Reliability investigation procedure for GaAs MMICs is proposed and test results for the S-band resistive feedback amplifier (μPG 100) are presented.

In order to elucidate what latent failure modes are and to investigate reliability levels for the developed MMIC, the MMIC is categorized into a several elements from the failure analysis points of view. The accelerated life tests have been conducted on process monitor samples, MMIC elements such as FETs, resistors, capacitors and the MMIC.

Device

It is essential to design the fundamental device structure from the reliability view point, in order to realize practical GaAs MMICs. The fundamental FET used in GaAs MMIC has a T-shaped WSi off-set gate structure overlayed with TiN-Pt-Au film to reduce the gate resistance. Figure 1 shows an FET cross-sectional view. WSi is adopted as Schottky material because of its high refractoriness. TiN is used as a barrier film against Au-diffusion in the gate metal system. The AuGe-Ni metal system is adopted as the ohmic contacts, while n^+ contact layers are also provided beneath the ohmic electrodes to suppress contact resistance degradation. Off-set gate FETs have high gate-to-drain breakdown voltage and low drain-to-source conductance. Si^+ ion implanation is used to form active layers, n^+ contact layers and resistors. The MIM structure is adopted in capacitors. In order to retain high wafer yield and reproducibility, all wafer fabrication process was performed using 10:1 stepper lithography.

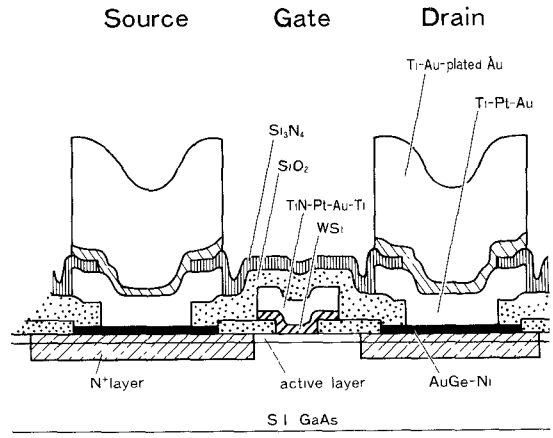

Fig.1 An FET cross-sectional view.

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Process Monitor Sample.

Basic evaluation items on process monitor samples are WSi Schottky junction reliability and ohmic contact reliability. In order to investigate WSi Schottky junction reliability itself, vertical structural diode test samples were fabricated and high temperature storage tests were carried out. The diode test sample cross-sectional view is shown in Fig. 2. Junction parameters, i.e., ϕB (barrier height) and n value (ideality factor) were very stable for 3000 hours even at Ta=337°C for 10 samples during the tests as shown in Fig.3. For the ohmic contact reliability investigation, contact resistance ρc degradation, accelerated by high temperature storage was evaluated. ρc was measured by using TLM (Transmission Line Model)[2] method. The results are shown in Fig. 4. Estimated MTF for contact resistance MTF at 130°C Tch is over 7 x 10^8 hours and ΔEa = 1.4 eV with a criterion of $\Delta\rho c = 5 \times 10\ \Omega\ cm^2$. This criterion corresponds to 10 % degradation in Rs (Source resistance) for the FET. As a result, it has been confirmed that WSi Schottky junction and ohmic contact have a superb potential for assuring GaAs MMIC reliability.

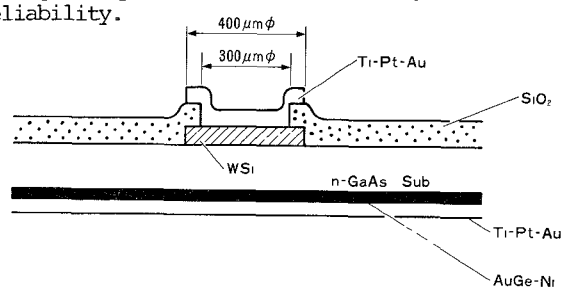


Fig.2 A diode test sample cross-sectional view.

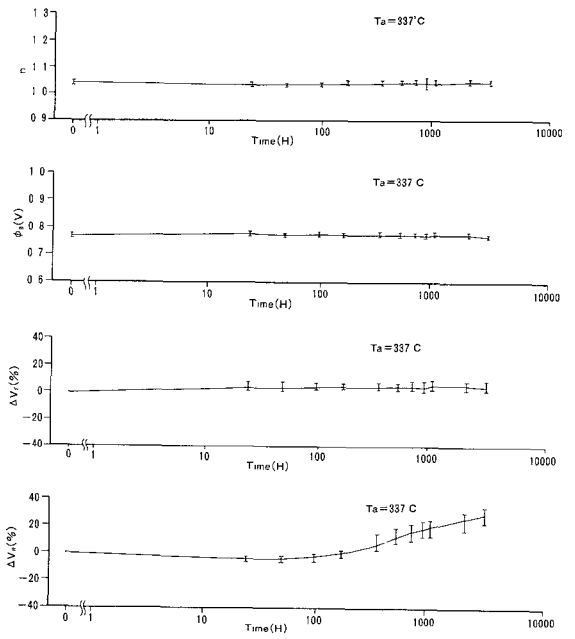


Fig.3 Schottky junction parameter changes on high temperature unbiased tests.

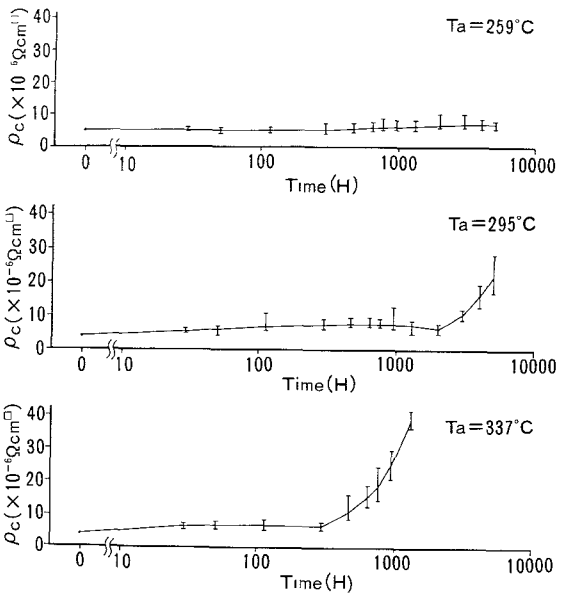


Fig.4 Ohmic contact resistance changes on high temperature unbiased tests.

MMIC elements

FET High temperature DC bias tests have been conducted on FETs at 240°C, 275°C and 300°C Tch value .

The biased test condition is V_{DS} = 8 V, $I_D \approx \frac{1}{2} I_{DSS}$ ($\approx$ 40 mA). High temperature storage tests have also been carried out at Ta = 295 °C and 337°C. Ten samples were tested in each stress level. The Arrhenius plots on the tests are shown in Fig. 5. Dominant failure modes for both biased and unbiased tests were the same. They were I_{DS} (specific drain current ; V_{DS} = 0.5 V, V_{GS} = 0 V), I_{DSS} and gm degradation. These are caused by series resistance increase. The Rs (source resistance) increase was virtually observed on degraded samples for both biased and unbiased tests. The changes in V_{th}, V_{GF}, ϕB and n , which depend on gate Schottky reliability, are little under both biased and unbiased tests. However the MTF for unbiased tests is longer than that for biased tests by more than one order. The MTFs for unbiased and biased tests are 8 x 10^8 hours and 3.5 x 10^7 hours, respectively at 130°C Tch. The possible series resistance increase cause for unbiased tests is ρc (contact resistance) degradation, because the MTF and ΔEa correspond to those of the ρc reliability test results approximately. On the other hand, for biased test condition, the series resistance increase is considered to be due to FET channel-narrowing effect originating from the surface depletion layer change at the interface between the passivation film and the active layer. This is recognized from the experimental result that the degraded samples got back almost the same characteristics when baked even at low temperature, such as 175°C for 24 hours. The estimated MTF for FET at Tch = 130°C

is over 3.5 x 10^7 hours for the bias condition of V_{DS} = 8 V, $I_D = \frac{1}{2} I_{DSS}$ with 10% degradation criteria.

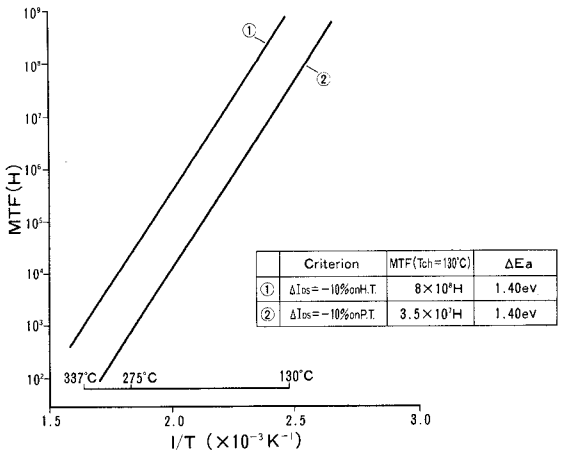


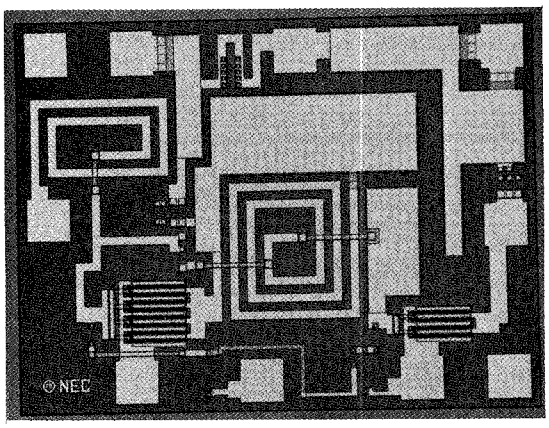
Fig.5 Arrhenius plots of 400 μm FETs on biased and unbiased tests.

Resistor High temperature DC biased and unbiased tests have been carried out on resistors at Tch = 275°C and 300°C. The ρ s (sheet resistance) for tested resistors, which were formed by Si ion implantation is 150 Ω/□ . The estimated resistor's MTF is over 1.3 x 10^8 hours for 7.5 V (E= 1.5 KV/cm) bias test condition with a criterion of 5 % resistance increase. The MTF for unbiased tests is longer than that for biased tests, which is probably due to almost the same reason as that for FET.

Capacitor Biased test on ten MIM capacitors, which are adopted a plasma-CVD SiN film as an insulator, has been performed with the bias condition of 8 V at Ta = 175°C for 2000 hours. No failure was observed.
Consequently, each element is considered to be sufficiently reliable for constructing MMICs.

MMIC

Accelerated life tests have been conducted for the S-band two-stage amplifiers. The tested IC (μPG100) is a resistive feedback amplifier, which has low noise figures (2.1 dB at 1.5 GHz) and flat gain up to 3 GHz. The gain variation from -25 to +75°C is suppressed within 0.6 dB by feedback and load resistors. The IC is hermetically sealed in newly developed ceramic packages suitable for surface mounting. The MMIC chip's top view and the equivalent circuit are shown in Fig. 6. The MMIC's typical characteristics and qualification test conditions are shown in Tables I and II, respectively. High temperature unbiased tests were performed for 3000 hours. The observed MTF for the MMIC is



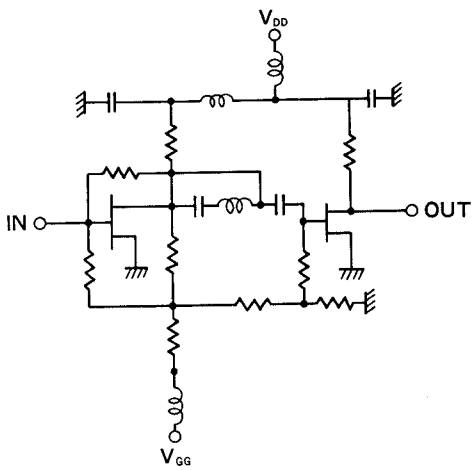


Fig.6 A wide band amplifier up to S-band chips top view and equivalent circuit.

1200 hours at 295°C with a criterion of 1.0 dB gain degradation. MTF at 130°C Tch is estimated to be 1.3 x 10 hours, using Ea = 1.4 eV, which is confirmed by the elements test results. The Arrhenius plots are shown in Fig. 7. RF operation life tests at Tch = 180°C and 205°C have also been conducted on 12 samples for each Tch value. Though severely excess RF input operation was involved in the tests, no failure has been observed for 3000 hours. NF and Ga changes during the tests are very small, as shown in Fig. 8. Thermal and mechanical environmental tests, based on MIL-STD-883 were carried out and no failure was observed.

Table 1
Typical Characteristics of GaAs MMIC

$Z_s=Z_L=50\Omega$ Ta=25 C $V_{DD}=5V$, $V_{GG}=-5V$

Parameter	Symbol	Test Condition	Typical Value
Drain Current	I_{DD}	Non input signal	40 mA
Gate Current	I_{GG}	Non input signal	−0 7 mA
Linear Gain	Ga	f=0 05~3GHZ	16 dB
Gain Flatness	ΔGa	f=0 05~3GHZ	±1 5 dB
Noise Figure	NF	f=0 05~3GHZ	2 7 dB
Output Power 1dB Compression	P_{1dB}	f=0 05~3GHZ	+6 dBm
Isolation	I_{SO}	f=0 05~3GHZ	40 dB
Input Return Loss	RL_{IN}	f=0 05~3GHZ	10 dB
Output Return Loss	RL_{OUT}	f=0 0 ~3GHZ	13 dB

Table 2
Life Test Conditions

Test		Test Condition			Sample Size
High Temperature Storage		Ta=227 C			10
		Ta=259 C			10
		Ta=295 C			10
High Temperature DC Bias Test		$V_{DD}=5V$ $V_{GG}=-5V$ $T_j=210$ C			10
High Temperature RF Operational Test		$V_{DD}=5V$ $V_{GG}=-5V$	$T_j=180$ C	Pin=−5dBm	4
				Pin=10dBm	8
			$T_j=205$ C	Pin=−5dBm	4
				Pin=10dBm	8
Thermal Environmental Test	Temperature Cycling Test	−65 C~175 C 200cycles			10
	Thermal Shock I	0 C~100 C 200cycles			10
	Thermal Shock II	−196 C~130 C 30cycles			10
Mechanical Environmental Test	Mechanical Shock	1500G, XYZ axis 5times 0 5ms			10
	Variable Frequency Vibration	100~2000HZ 20G XYZ axis 4times 4min			
	Constant Acceleration	20000G XYZ axis 1min			

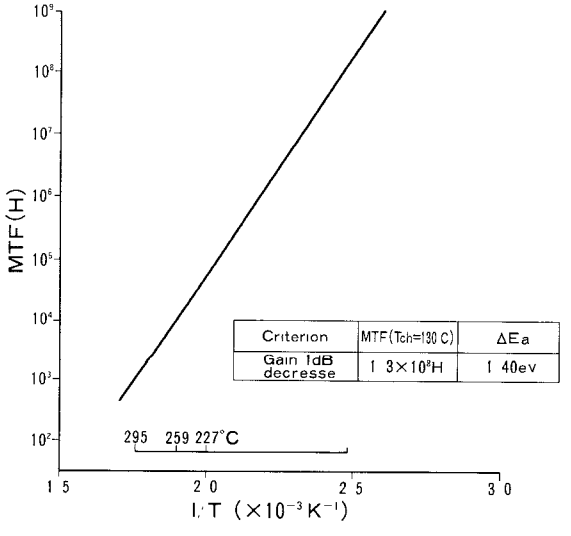


Fig.7 Arrhenius plots of a wide band amplifier up to S-band on high temperature unbiased tests.

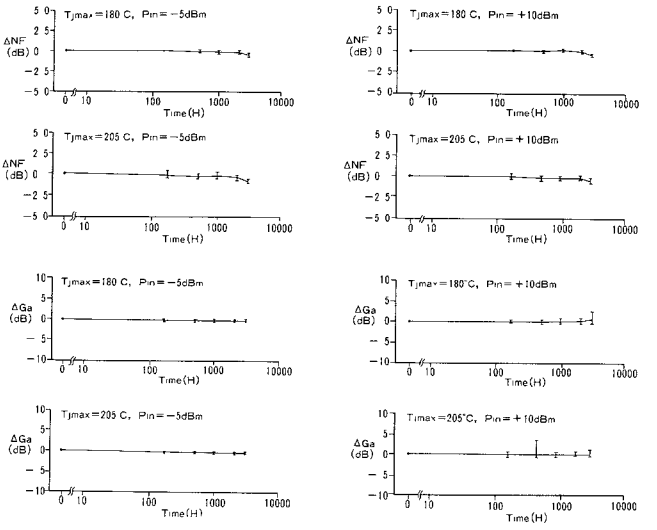


Fig.8 High temperature RF operation test results for a wide band amplifier up to S-band.

Radiation Hardness

Gamma-ray irradiation tests were carried out for S-band two-stage amplifier , two-modulus prescalers and their FETs. Dose rate is about 1 x 10^6 rad/hour. Figure 9 shows FET's DC parameter changes under the tests. As clearly shown in the figure, the DC parameters changes for FETs are less than 5 % up to 10^7 rad and there was a peak in gm and I_{DSS} at around 10^7 rad. The degradation for over 10^7 rad range is considered to be due to GaAs bulk damage caused by gamma ray irradiation. Figure 10 shows I_{DD} and $|S_{21}|$ changes in the S-band two stage amplifiers under the tests. Both DC and RF characteristics are more stable up to 10^7 rad than FET parameters themselves becauce of the IC's feedback effect. The same tests were carried out on the low power dissipated 128/129 two modulus GaAs prescaler IC for use in a hand-held mobile telephone or a cellular system, implemented by a shallow depletion type SCFL gate. Figure 11 shows the chip top view. Figure 12 shows how the IC currents varied with increasing radiation dose, where the devices were biased to give (A) sufficient current drivability and (B) functional minimum current. As clearly shown in the figure, only 5 % increase and 15 % decrease were observed in case (A) and (B), respectively at around 10^7 rad. This is because there was a peak in gm for FETs at this irradiation region. Consequently, it was confirmed that the MMICs are sufficiently tough from the view point of radioation hardness.

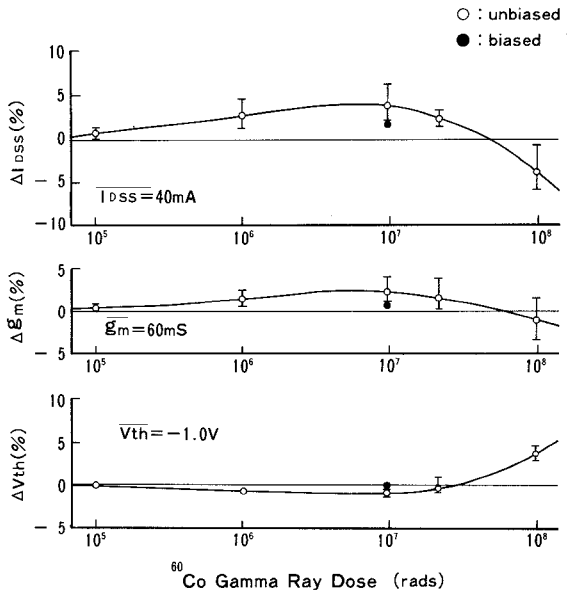


Fig.9 Gamma-ray irradiation test results for a FET.

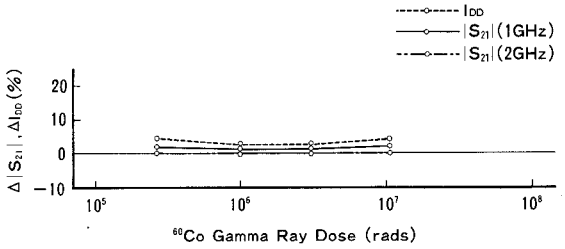


Fig.10 Gamma-ray irradiation test results for a wide band amplifier up to S-band.

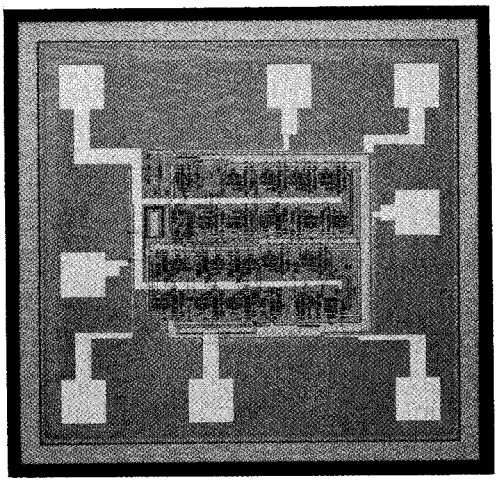


Fig.11 A two modulus prescaler chip top view.

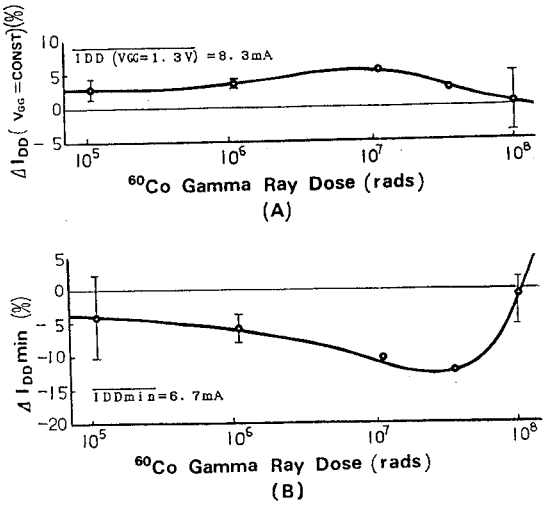


Fig.12 Gamma-ray irradiation test results for a two modulus prescaler IC.
A; Change in I_{DD}, where the devices were biased to give sufficient drivability.
B; Change in I_{DD}, where the devices were biased to give functional minimum current.

Conclusion

Accelerated life tests have been performed on S-band two-stage amplifiers, their FETs and process monitor samples. 0.35 to 1.3 x 10^8 hours MTF at 130°C Tch was estimated. Radiation hardness tests have been carried out on the FETs, S-band two-stage amplifiers and two modulus prescalers. No degradation was observed up to 10^7 rad gamma ray irradiation with 5% criteria for the MMICs and FETs. It has been confirmed that the MMICs, produced using NEC's 0.8 μm long T-shaped WSi gate FET manufacturing process are sufficiently reliable for practical applications.

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